## WHAT IS CLAIMED IS:

1	1. A semiconductor device comprising:		
2	a substrate;		
3	a gate region on top of the substrate;		
4	a first and second sidewall liners situated on a first and second sides of the		
5	gate region respectively, the first and second sidewall liners having a vertical		
6	part contacting sidewalls of the gate region and a horizontal part contacting the		
7	substrate; and		
8	a first and second recessed spacers situated on top of the first and second		
9	sidewall liners respectively,		
10	wherein a height of the first and second recessed spacers is lower than a		
11	height of the sidewall liner, and		
12	wherein the horizontal part of each sidewall liner is shorter than the		
13	corresponding recessed spacer on top thereof.		
1	2. The device of claim 1 wherein the height of the recessed spacer is at		
2	least 50 Å lower than the height of the vertical part of the sidewall liner.		
1	3. The device of claim 1 wherein the horizontal part of each gate		
2	sidewall liner is at least 10 Å shorter than the recessed spacers.		
1	4. The device of claim 1 wherein the gate region further includes a		
2	gate dielectric and electrode layers.		

1	5. exceed 1800 <i>A</i>	The device of claim 4 wherein the height of the gate region does not $ m \AA$ .
1	6.	The device of claim 1 wherein the recessed spacer is SiN based.
1 2	7. Ge, Ar, or O <sub>2</sub>	The device of claim 1 wherein the recessed spacer further includes based impurities.
1	8.	The device of claim 1 wherein the sidewall liner is oxide based.
1	9.	The device of claim 1 further comprising a contact etching stopper
2	(CES) layer f	ormed over the recessed spacer with a predetermined stress level.
1 2	10. stress.	The device of claim 9 wherein the CES layer imposes a compressive
1	11. stress.	The device of claim 9 wherein the CES layer imposes a tensile
1 2	12. stopper layer	The device of claim 9 wherein the stress level of contact etching r is larger than 200M Pa.
1 2	13. smaller than	The device of claim 9 wherein the thickness of the CES layer is 600Å.

A method for fabricating at least one semiconductor device having

1

14.

4

5

gate region.

a gate region and recessed spacers, comprising:		
forming a substrate;		
forming a gate region on top of the substrate, the gate region having a gate		
electrode and a gate dielectric region;		
forming two sidewall liners confining the gate region therebetween;		
forming two spacers on top of the sidewall liners on both sides of the gate		
region, a height of the spacers matching substantially a height of the sidewall		
spacers;		
reducing the width of the sidewall liners underneath the spacers to pull		
back from an edge of each spacer by a predetermined distance; and		
forming two recessed spacers by reducing the height of the formed		
spacers,		
wherein the reduced spacer height reduces device channel stress.		
15. The method of claim 14 wherein the forming two spacers further		
includes depositing spacer material and etching the deposited spacer material so		
that the top of the spacers slope down from the top of the sidewall liners to a		

horizontal part of the sidewall liner that extends along the substrate from the

1	16.	The method of claim 14 wherein the reducing further includes:	
2	forming an oxide layer over the spacers, the sidewall liners, and the gate		
3	region;		
4	etchi	ng the oxide off within a predetermined time period so that the width	
5	of the sidewall liners are pulled back for a predetermined distance.		
1	17.	The method of claim 14 wherein forming two recessed spacers	
2	further inclu	ides selectively etching the spacers to reduce at least 50Å in the	
3	height of the	e spacers to form the recessed spacers.	
1	18.	The method of claim 14 further comprising introducing one or	
2	more impur	ities to the spacers to further reduce the device channel stress.	
1	19.	The method of claim 14 wherein the predetermined distance pulled	
2	back from th	ne edge of each spacer is at least 10Å.	
	•		
1	20.	The method of claim 14 further comprising forming a contact etch	
2		layer over the recessed spacers for further modifying the device	
3	channel stre	SS.	
1	21		
1	21.	The method of claim 20 wherein the CES layer imposes a	
2	compressive	e stress.	
1	22.	The method of claim 20 wherein the CES laver impresses a travelle	
		The method of claim 20 wherein the CES layer imposes a tensile	
2	stress.		

23. A transistor comprising:		
a substrate;		
a gate electrode on top of the substrate;		
a first and second "L" shaped gate sidewall liners confining the gate		
electrode therebetween, the first and second sidewall liners having a vertical par		
contacting sidewalls of the gate electrode and a horizontal part contacting the		
substrate; and		
a first and second recessed spacers situated on top of the first and second		
sidewall liners respectively; and		
a contact etching stopper (CES) layer situated over the recessed spacers,		
wherein a height of the first and second spacers is lower than a height of		
the gate sidewall liners and a width of the gate sidewall liners is shorter than that		
of the first and second spacers, and		
wherein the recessed spacers are doped with predetermined impurities		
for modifying a channel stress of the transistor.		
24. The transistor of claim 23 wherein the recessed spacers are at least		
50 Å lower than the gate sidewall liners.		

The transistor of claim 23 wherein the gate sidewall liners are at

The transistor of claim 23 wherein the impurities doped into the

SF\\(\text{39956.3}\) - 16 -

recessed spacers includes Ge, Ar, or O<sub>2</sub> based impurities.

least  $10\mbox{\normalfont\AA}$  shorter than the recessed spacers.

1

2

1

2

25.

26.

1	27.	The transistor of claim 23 wherein the CES layer formed over the
2	recessed sna	cers is thicker than the recessed spacers.

- 1 28. The transistor of claim 23 wherein the contact etching stopper layer 2 is thinner than 600Å.
- 1 29. The transistor of claim 23 wherein the contact etching stopper layer 2 imposes a tensile stress less than 1.5G Pa.
- 1 30. The transistor of claim 23 wherein the contract etching stopper 2 layer imposes a compressive stress less than 1.0G Pa.
- 1 31. A semiconductor device comprising:
- 2 a substrate;
- 3 a gate region on top of the substrate;
- 4 two sidewall liners situated on two sides of the gate region; and
- 5 a spacer situated on top of each sidewall liner,
- 6 a contact etching stopper layer over the spacers,
- 7 wherein the contact etching stopper layer is thicker than the spacer.
- 1 32. The device of claim 31 wherein the thickness of contact etching 2 stopper layer is smaller than 600 Å.
- 1 33. The device of claim 31 wherein the contact etching stopper layer 2 imposes tensile stress.

1	34.	The device of claim 33 wherein a stress level of the contact etching
2	stopper laye	r is less than 1.5G Pa.

- 1 35. The device of claim 31 wherein the contact etching stopper layer 2 imposes compressive stress.
- 1 36. The device of claim 35 wherein a stress level of the contact etching 2 stopper layer is less than 1.0G Pa.
- 1 37. A semiconductor device comprising:
- 2 a substrate;
- 3 a gate region on top of the substrate;
- 4 two "L" shaped sidewall liners situated on two sides of the gate region;
- 5 a recessed spacer situated on top of each sidewall liner; and
- 6 a contact etching stopper layer formed over the spacers, the sidewall, and
- 7 the gate region,
- 8 wherein the contact etching stopper layer is thicker than the spacer, and
- 9 wherein the sidewall liner is higher and wider than the recessed spacer.
- 1 38. The device of claim 37 wherein the thickness of the contact etching 2 stopper layer is smaller than 600 Å.
- 1 39. The device of claim 37 wherein the contact etching stopper layer 2 imposes a tensile stress.
- 1 40. The device of claim 39 wherein a stress imposed by the contact 2 etching stopper layer is less than 1.5G Pa.

[TSMC2003-0025]

- 1 41. The device of claim 37 wherein the contact etching stopper layer
- 2 imposes a compressive stress.
- 1 42. The device of claim 41 wherein a stress imposed by the contact
- 2 etching stopper layer is less than 1.0G Pa.

SF\39956.3 - 19 -